

Fig. 7. Power conversion efficiency versus frequency for (a) hyperabrupt (5F1) and (b) abrupt (5M4) Schottky-barrier varactors where  $P_{IN}$  is maintained at 50 mW.

the mount geometry and average diode capacitance for the two cases evaluated.

It should be pointed out that, at this stage in harmonic generator development at 230 GHz, the losses of the mount dominate the losses of the varactor. Thus, a more efficient varactor would be expected to yield only small improvements in the performance of the frequency multiplier.

#### VII. SUMMARY

The models developed to predict the electrical parameters of a hyperabrupt varactor based on its physical parameters were shown to be accurate. Reverse breakdown voltage, capacitance, and series resistance were examined as a function of the impurity doping profile, epitaxial layer thickness, and anode size.

Hyperabrupt junction devices were shown to have superior dc characteristics when compared to an equivalent abrupt junction device. The 5F1 devices exhibited higher breakdown voltages, lower series resistance, and a greater capacitance modulation than an optimized abrupt junction diode. Comparison of the behavior of 5M4 and 5F1 devices mounted in a 190–230-GHz doubler showed that the 5F1 had a larger output power bandwidth integral, and a peak efficiency at a higher frequency than the 5M4. The RF performance on both abrupt and hyperabrupt devices was limited by the characteristics of the microwave circuit.

The design, fabrication, and testing of devices in this research was aimed at competing directly with an optimized abrupt junction device in an application for which it has established its desirability. To facilitate the development of higher order frequency multipliers, with harmonic outputs of order 3 and higher, and usable output power, there is a need for devices with high breakdown voltages (25–30 V), which can handle higher pump powers, but still have a high degree of capacitance modulation. Fig. 2 indicates that the hyperabrupt structures show promise at being able to satisfy this need.

It is possible to reduce device series resistance by allowing punch-through breakdown to occur. Capacitance modulation and maximum breakdown voltage may be sacrificed to gain conversion efficiency by the reduction of power dissipation in the device.

#### VIII. CONCLUSION

The use of a hyperabrupt junction varactor diode for millimeter-wave applications was shown to be successful. Device com-

parison showed the hyperabrupt device to perform, in general, at least as well as the equivalent abrupt junction device. At present, the microwave circuit limits the performance of frequency multipliers in the 100–230-GHz output frequency range. However, with continued improvement in mount design, it is expected that the hyperabrupt device will yield superior conversion efficiency and power handling capabilities when compared with the abrupt junction devices in the same improved mount.

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#### A Limiter for High-Power Millimeter-Wave Systems

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**Abstract**—A high-power limiter for use in millimeter-wave systems has been designed and demonstrated. The RF control is provided by an array of p-i-n diodes fabricated into the surface of a high-resistivity silicon window. Orientation-dependent etching of the silicon is used to build diodes with parallel injection surfaces. The window is mounted into the waveguide using a metal membrane which simplifies construction and lowers cost.

#### I. INTRODUCTION

In high-power communication and radar systems, power limiter components are used in front of the mixer diode for RF burnout protection. Typically, a limiter may need to provide 20–50-dB attenuation for high-level signals while minimum possible loss is desired for low-level signals. In addition, if the limiter is of the

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reflection type, it can be used to switch the antenna from the receiver to the transmitter during transmission.

Limiter elements have been built in the past using various phenomena such as gaseous breakdown, magnetic resonance, and p-i-n diodes. For the small dimensions of the millimeter-wave system, the limiter component was designed using an array of p-i-n diodes. This array is fabricated on the surface of a silicon wafer which is placed across the waveguide normal to the propagation axis. The size of the silicon element is comparable to that of the waveguide, which provides the double benefit of a) high-power capability and b) fabrication ease.

Switches using arrays of p-i-n diodes on a silicon window have been fabricated previously for operation at lower frequencies. The initial work of Mortenson *et al.* [1] produced single-pole single-throw switches which exhibited waveguide bandwidth at X-band, insertion loss below 1 dB, isolation of 20 dB, peak power over 200 kW, average power of hundreds of watts, and speed of several microseconds. In subsequent works, Armstrong and Bakeman [2] demonstrated octave bandwidth with switching speed below 50 ns, and Anand, Armstrong, *et al.* [3], demonstrated double-throw operation.

The current work extends the semiconductor window component to operation at millimeter-wave frequencies.

## II. DESIGN

High-power limiting is provided by placing a semiconductor window control element across the waveguide. Fabricated into one surface of this window is a matrix of p-i-n diodes. In the unbiased state, these diodes appear as a shunt capacitance across the waveguide. In the biased conducting state, the diodes produce a large admittance across the path of the millimeter wave.

The capacitance value of the unbiased window is a function not only of the capacitance of the individual diodes but also of the series/parallel configuration of the diode array. For example, in the conceptual sketch of Fig. 1, there are 2 diodes in series in each of the 2 parallel columns yielding a new capacitance equal to that of one diode. The advantage of this arrangement is an increased power capability for a fixed capacitive loading. The cost or tradeoff for the power increase is increased control bias current.

To provide high-quality p-i-n diodes and greater design freedom, the p-i-n diode array is fabricated into, rather than onto, the surface of the silicon window. Silicon is etched away from one surface so as to leave rectangular ridges of silicon. Parallel faces on the sides of these ridges are realized by using an orientation dependent etchant on (110)-oriented silicon. The opposing side faces are doped with phosphorous or boron to produce p-i-n diode bars. The hollow spaces between the ridges are back-filled with gold. These gold channels are used as conductors for the control bias current (see Fig. 2).

A typical pattern used for component fabrication is shown in Fig. 3(a) and (b). Eight diodes with 20- $\mu\text{m}$  *I*-regions are stacked in each of five columns. This gives a total of 40 diodes on the window. Other patterns used have 12 diodes in a column and/or 14- $\mu\text{m}$  *I*-region widths.

The diode columns were placed only in the central portion of the window for two reasons: 1) to reduce the total number of diodes and the associated bias current; and 2) to facilitate the fabrication of an inductive iris. The inductive iris partially compensates the capacitance of the diodes, bias conductors, and substrate silicon.

For 20- $\mu\text{m}$ -wide diodes, the ambipolar diffusion length only needs to be about 10  $\mu\text{m}$  [4]. Accordingly, the excess carrier

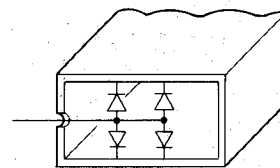


Fig. 1. Conceptual window control element.

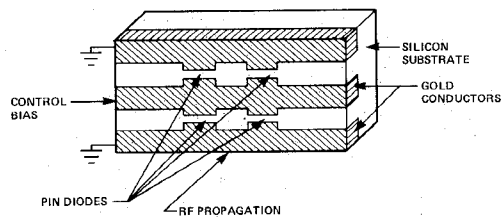


Fig. 2. Window control element with four diodes.

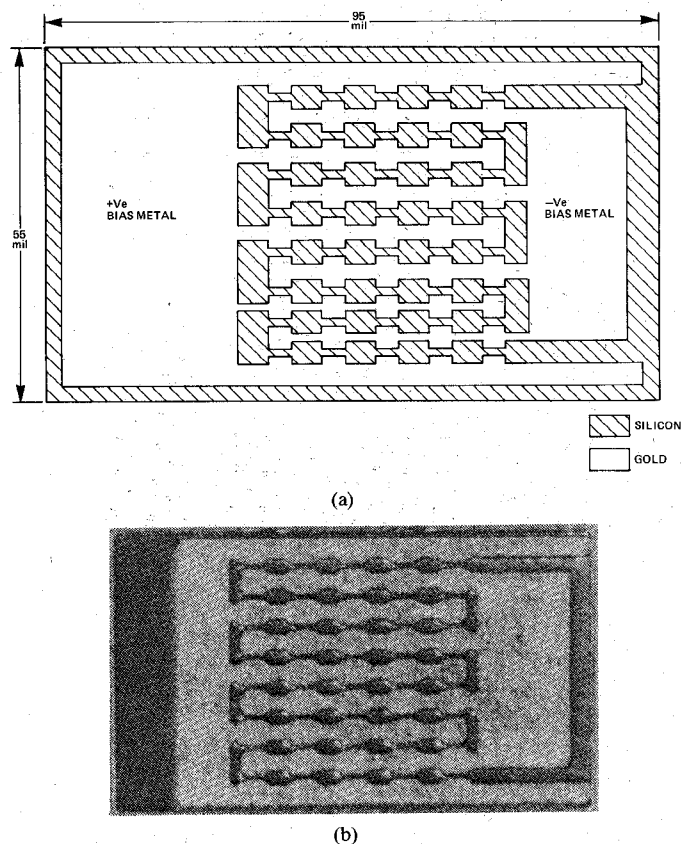


Fig. 3. (a) Schematic of millimeter silicon bulk window limiter element. (b) Millimeter silicon bulk window limiter element.

lifetime in the silicon after processing can be as low as 100 ns, which should not be a problem. This assumes that the predominant loss of carriers is by recombination and not by flow out the sides of the diode. To minimize loss of carriers to the bulk, the diode (etch) depth should be equal to and preferably greater than the separation of the p and n regions.

The control bias current is distributed to the diodes by conductive rows which connect to a common bias pad on one end of the sample. A single-wire lead is bonded to this pad for external connection. The return current path from the diodes is through the conductive channel which surrounds the diode array on the other three edges. This channel is directly connected to the waveguide wall by the mounting structure.

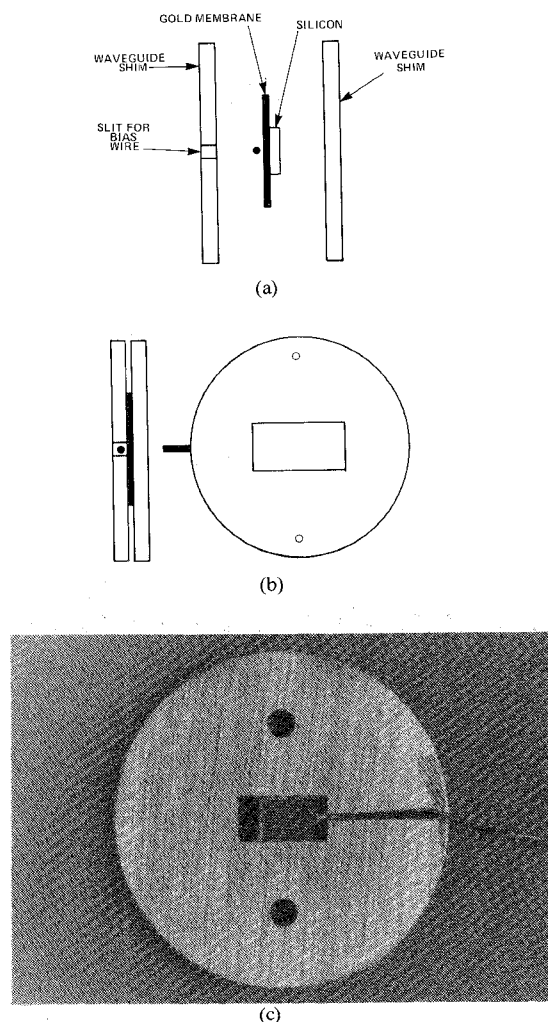


Fig. 4. (a) Parts—Single window test mount. (b) Assembly—Single window test mount. (c) Millimeter silicon bulk window limiter.

A bias current of about 200 mA per window is required for the desired RF isolation. This current, as well as a turn-on spike, is to be provided by a driver which is triggered by either a logic signal from the transmitter modulator, or a low-level detector signal. The detector is placed in front of the window switch to detect the presence of high-level external signals. It is coupled to the main waveguide through a 40-dB coupler for its own protection. Protection for the receiver is thus provided from both the system transmitter and foreign signals.

### III. FABRICATION

The starting material for the window elements is high resistivity  $3500\text{-}\Omega\cdot\text{cm}$  (110)-oriented silicon. The silicon wafers are thermally oxidized (5000 Å). Channels are defined by standard lithographic methods and etched in the oxide. The wafer is immersed in a silicon etch preferential to the (110) plane so that channels 25  $\mu\text{m}$  deep with straight side walls are etched into the silicon. The original oxide is stripped, and a new oxide is grown. Diode regions are defined and etched in alternating channels and boron is diffused into these channels. A 7000-Å layer of silicon dioxide is deposited and the undoped channels are etched open. These are doped by diffusing phosphorous. The resulting structure is an array of lateral p-i-n diodes. All oxides are removed and the wafer is metallized by sputtering titanium-gold. Extra gold is electroplated to fill up the channels completely. The

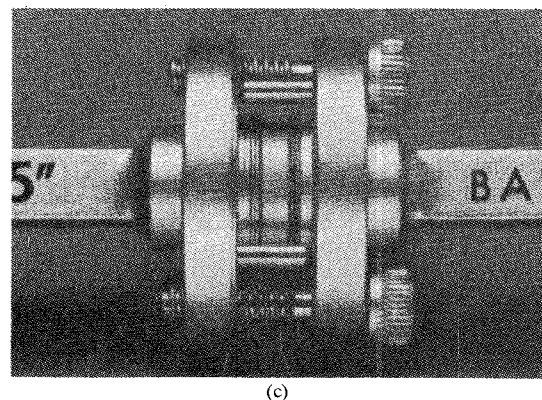
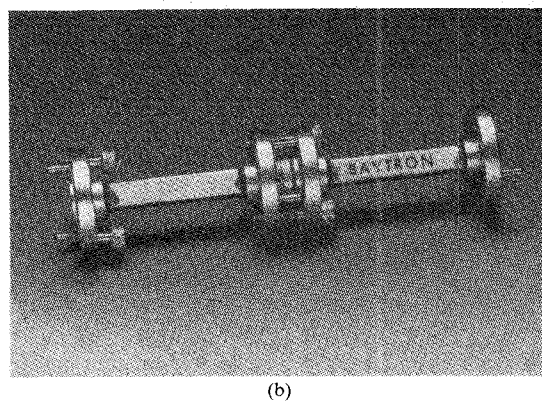
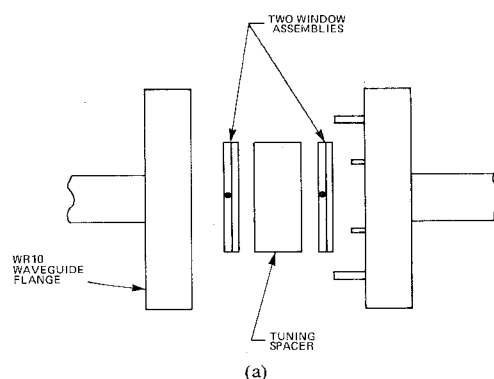


Fig. 5. (a) Tuned dual window limiter. (b) Millimeter dual window limiter. (c) Close up view of millimeter dual window limiter.

excess gold is lapped/polished away to leave a flat surface. The wafer is backside lapped (100  $\mu\text{m}$ ) to reduce the thickness of the device, and cut by diamond saw to fit into the waveguide mount.

### IV. MOUNTING

At higher frequencies, metallic RF losses become increasingly important due to reduced conduction skin depth and difficult machining tolerances. The best mounting and tuning structures are usually those that are mechanically simple and produce minimal disturbance to the RF field pattern. The windows are mounted into standard waveguide by means of a gold membrane. A 2-mil-thick gold membrane with an opening to expose the diode array is bonded or soldered to the periphery of the silicon window chip. The window is placed into the waveguide (or a slice of guide) and the gold membrane is clamped between two waveguide flanges. The structure used in the program employed waveguide shimstock pieces, as shown in Fig. 4 to facilitate the handling of several part types. This proved to be a low-loss and

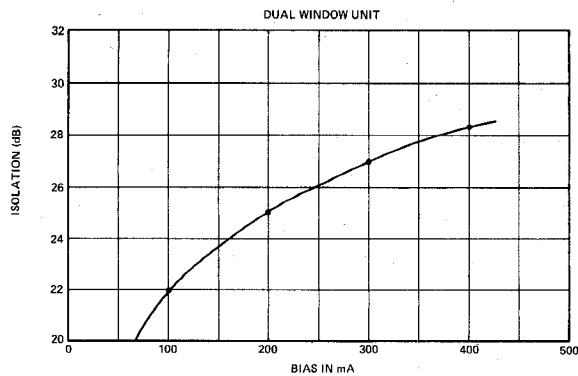


Fig. 6. Isolation versus dc bias for dual unit no. 2.

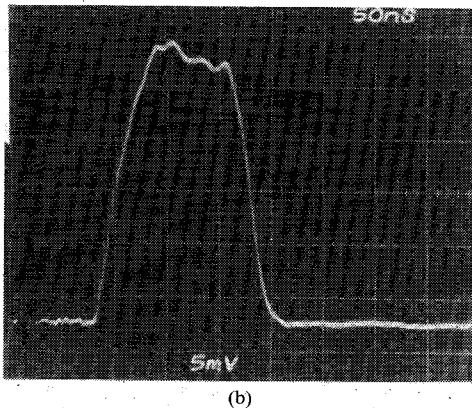
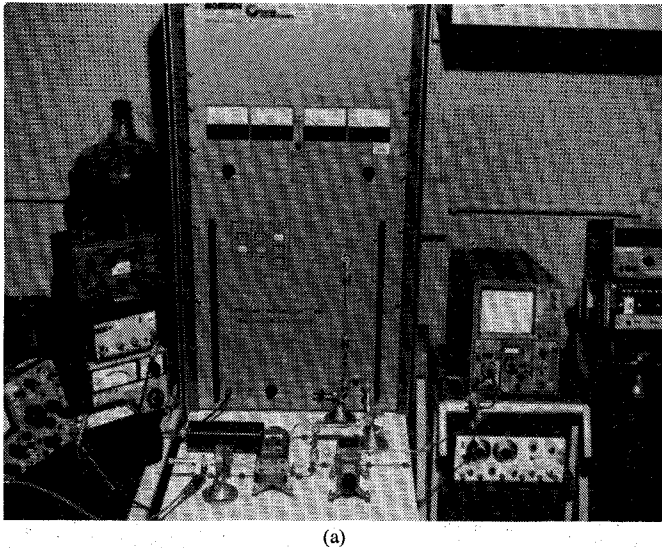


Fig. 7. (a) Millimeter-wave high-power test system. (b) RF pulse from millimeter-wave high-power test system.

flexible mounting structure. The insertion loss measured for a stack of 1 to 5 shimstocks (each 0.23 mm thick) inserted between 2 flanges was insignificant (under 0.2 dB). The return loss was 24

dB for 1 shim and dropped to a minimum of 17 dB for 4 shims (about  $1/4$  wavelength) [5]. Small holes in the shims allowed the use of alignment pins in the flanges.

## V. MEASUREMENTS

The RF insertion-loss and return-loss measurements were taken on individual window elements as well as tuned pairs. Considering the individual window as a shunt combination of a variable conductance ( $G$ ) in parallel with a fixed capacitive susceptance ( $B$ ), typical zero bias values of  $G/Y_0$  and  $B/Y_0$  are 0 to 0.2, and 2 to 3, respectively.

Tuning of the capacitive susceptance was achieved by placing in the waveguide two window elements separated by a little over one-half wavelength so that the susceptances cancelled (see Fig. 5). Taking into consideration the holder dimensions and the silicon thickness, the length of the waveguide spacer section needed is only about 0.16 cm (62 mil).

The RF performance measured for the initial units was 1.6-dB insertion loss with no bias and 26-dB isolation at 400-mA bias. The isolation is a continuous function of bias increasing about 3 dB for each doubling of the current (see Fig. 6).

The bandwidth is approximately 3 GHz and exceeds the 1-GHz value sought. High-power testing was done at the USA-ERADCOM facilities at Fort Monmouth, NJ. The high-power test system basically consisted of a Varian EIO and a modulator (see Fig. 7) built by Norden to generate 0.1- $\mu$ s pulses up to 1.5 kW of peak power. As a limiter control element, the window would see high power only during the biased condition. Accordingly, the window elements (single and dual) were biased and exposed to peak powers up to 875 W with no observed arcing or degradation.

The average power capability was not measured; however, the thermal resistance calculated is 10 to 15°C/W dissipated. For a switching operation, less than 20 percent of the incident power is dissipated. Thus, considerable average power can be handled.

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